Amendment to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A method for forming a storage node of a capacitor in a semiconductor device, the method comprising:

forming a first amorphous silicon layer doped with a first doping concentration, the first doping concentration being of a dose to suppress dopants from locally agglomerating;

forming a second amorphous silicon layer that is substantially undoped on the first amorphous silicon layer in an in-situ condition;

patterning the first amorphous silicon layer and the second amorphous silicon layer to form a first storage node;

converting the second amorphous silicon layer to form a plurality of silicon grains on an inner wall of the first amorphous silicon layer, wherein substantially all of the second amorphous silicon layer is converted to the silicon grains; and

doping the first storage node and the silicon grains with dopants until a second doping concentration is reached, the second doping concentration being of sufficient dosage to provide requisite conductivity to the first storage node,

wherein a dielectric layer is formed over the doped first storage node and a second storage node is formed over the dielectric layer.

2. (Previously Presented) The method as recited in claim 1, wherein the first doping concentration ranges from about $1 \times 10^{19}/cm^3$ to about $9 \times 10^{19}/cm^3$ and the second doping concentration ranges from about $24 \times 10^{20}/cm^3$ to about $1 \times 10^{22}/cm^3$.

3. (Previously Presented) The method as recited in claim 1, wherein the first doping concentration ranges from about $1 \times 10^{19}/cm^3$ to about $9 \times 10^{19}/cm^3$ and the second doping concentration ranges from about $24 \times 10^{20}/cm^3$ to about $1 \times 10^{22}/cm^3$, wherein the step of

doping the first storage node and the silicon grains involves a chamber plasma doping method in an atmosphere containing phosphorus.

4. (Previously Presented) The method as recited in claim 3, wherein the chamber plasma doping is performed at a temperature ranging from about 700 °C to about 800 °C and a pressure ranging from about 1.5 torr to about 2.5 torr for about 2 minutes and about 5 minutes by supplying a plasma power ranging from about 300 W to about 500 W and phosphine (PH_3) flowed with a quantity of about 300 sccm to about 500 sccm.

5. (Original) The method as recited in claim 1, wherein the step of doping the impurity onto the storage node and the silicon grains proceeds by performing another doping method of a furnace annealing in an atmosphere of a gas containing phosphorus.

6. (Original) The method as recited in claim 5, wherein the furnace annealing is performed at a temperature in a range from about 600 °C to about 750 °C and a pressure ranging from about 5 torr to about 10 torr for about 1 hour to about 2 hours by flowing PH_3 gas with a quantity ranging from about 100 sccm to about 200 sccm.

7. (Original) The method as recited in claim 1, wherein the step of doping the impurity onto the storage node and the silicon grains further includes the steps of:

performing a chamber plasma doping in an atmosphere of a gas containing phosphorus; and

diffusing the doped impurity through a furnace annealing.

8. (Original) The method as recited in claim 7, wherein the chamber plasma doping is performed at a temperature ranging from about 700 °C to about 800 °C and a pressure ranging from about 1.5 torr to about 2.5 torr for about 1 minute and about 5 minutes by supplying a plasma power in a range from about 300 W to about 500 W and PH_3 gas flowed with a quantity ranging from about 100 sccm to about 500 sccm.

9. (Original) The method as recited in claim 7, wherein the furnace annealing is performed at a temperature ranging from about 600 °C to about 750 °C and a pressure ranging from about 5 torr to about 10 torr in an atmosphere of nitrogen for about 1 hour to about 2 hours.

10. (Previously Presented) The method as recited in claim 1, wherein the converting step further includes the step of cleaning the surface of the first storage node on which the silicon grains are formed.

11. (Previously Presented) The method as recited in claim 10, wherein the step of cleaning the surface of the first storage node proceeds by using a wet chemical such as hydrogen fluoride (HF) and buffered oxide etchant (BOE).

29. (Previously Presented) A method for forming a storage node of a capacitor in a semiconductor device, the method comprising:

providing a trench on a substrate;

forming a first amorphous silicon layer doped with a first doping concentration within the trench, the first amorphous silicon layer having inner and outer walls, the inner wall defining a space within the trench, the first doping concentration ranging from about 1 x $10^{19}/cm^3$ to about 2 x $10^{20}/cm^3$ to suppress dopants from locally agglomerating;

forming a second amorphous silicon layer that is substantially undoped on the first amorphous silicon layer in an in-situ condition;

patterning the first amorphous silicon layer and the second amorphous silicon layer to form a first storage node;

converting the second amorphous silicon layer to form a plurality of silicon grains on the inner wall of the first amorphous silicon layer, wherein substantially all of the second amorphous silicon layer is converted to the silicon grains;

converting the first amorphous silicon layer to a polysilicon layer; and

doping the first storage node and the silicon grains with dopants until a second doping concentration is reached, the second doping concentration being of sufficient dosage to provide requisite conductivity to the first storage node,

wherein a dielectric layer is formed over the first storage node and a second storage node is formed over the dielectric layer and within the space defined in the trench.

30. (Previously Presented) The method as recited in claim 29, the first doping concentration ranging from about 1 x $10^{19}/cm^3$ to about 9 x $10^{19}/cm^3$.

31. (Previously Presented) The method as recited in claim 30, wherein and the second doping concentration ranges from about 24 x $10^{20}/cm^3$ to about 1 x $10^{22}/cm^3$.

32. (Previously Presented) The method as recited in claim 30, wherein the doping step involves a chamber plasma doping in a phosphorus atmosphere.

33. (Previously Presented) The method as recited in claim 30, wherein the chamber plasma doping is performed at a temperature ranging from about 700 °C to about 800 °C and a pressure ranging from about 1.5 torr to about 2.5 torr for about 2 minutes and about 5 minutes by supplying a plasma power ranging from about 300 W to about 500 W and phosphine (PH_3) flowed with a quantity of about 300 sccm to about 500 sccm.

34. (Previously Presented) The method as recited in claim 30, wherein the converting step further includes the step of cleaning the surface of the first storage node.

35. (Previously Presented) The method as recited in claim 34, wherein the step of cleaning the surface of the first storage node involves using a wet chemical such as hydrogen fluoride (HF) and buffered oxide etchant (BOE).

36. (Previously Presented) A method for forming a storage node of a capacitor in a semiconductor device, the method comprising:

providing a trench on a substrate;

forming a first amorphous silicon layer doped with a first doping concentration within the trench, the first amorphous silicon layer having inner and outer walls, the inner wall defining a space within the trench, the first doping concentration being of a dosage to suppress dopants from locally agglomerating;

forming a second amorphous silicon layer that is substantially undoped on the first amorphous silicon layer in an in-situ condition;

patterning the first amorphous silicon layer and the second amorphous silicon layer to form a first storage node;

converting the second amorphous silicon layer to form a plurality of silicon grains on the inner wall of the first amorphous silicon layer, wherein substantially all of the second amorphous silicon layer is converted to the silicon grains;

converting the first amorphous silicon layer to a polysilicon layer; and

doping the first storage node and the silicon grains with dopants until a second doping concentration is reached, the second doping concentration being of sufficient dosage to provide requisite conductivity to the first storage node,

wherein a dielectric layer is formed over the first storage node and a second storage node is formed over the dielectric layer and within the space defined in the trench.